SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY:: PUTTUR
(AUTONOMOUS)
B.Tech II Year I Semester Supplementary Examinations June-2024
DIGITAL SYSTEM DESIGN
(Electronics and Communication Engineering)

Time: 3 Hours   **Max. Marks: 60**

PART-A
(Answer all the Questions 5 x 2 = 10 Marks)

1	a	Convert decimal 27.315 to binary.	CO1	L1	2M
	b	Minimize the following Boolean function using K-map $F(A, B, C, D) = \Sigma m(1,4,5,6,12,13,14,15)$.	CO1	L1	2M
	c	Compare Synchronous and Ripple counters.	CO2	L2	2M
	d	Briefly Explain about ECL.	CO2	L2	2M
	e	Explain the structure of a VHDL program.	CO5	L2	2M

PART-B
(Answer all Five Units 5 x 10 = 50 Marks)

UNIT-I

2	a	Perform the following subtraction using 9's complement for the given. i) 54321-41245 ii) 1231-4145	CO1	L1	5M
	b	Subtraction by using 1's complement for the given. i) 111011-110110 ii) 10001-10011	CO1	L1	5M

OR

3	a	Express the Boolean function F= A+B'C as a sum of minterms.	CO1	L1	5M
	b	Express the Boolean function F= XY+X'Z as a product of maxterm.	CO1	L1	5M

UNIT-II

4		Simplify the following Boolean function for minimal SOP & POS form using K-map. i) $F(A, B, C, D) = \Sigma (0,1,2,5,8,9,10)$ ii) $F(A, B, C, D) = \pi(1,3,5,7,12,13,14,15)$.	CO3	L2	10M

OR

5	a	Implement the following Boolean function using 4:1 Multiplexer. $F(A, B, C) = \Sigma (1,2,6,7)$.	CO4	L3	5M
	b	Design a 1:4 Demultiplexer and mention the applications of a DEMUX.	CO4	L1	5M

UNIT-III

6	a	Draw the logic diagram of a JK – flip flop and explain its operation.	CO3	L4	5M
	b	What is the need for Master Slave JK FF and explain its operation with neat diagrams.	CO3	L2	5M

OR

7	a	Design a Positive edge triggered Master-Slave D flip flop.	CO3	L2	4M
	b	Design and implement a BCD Ripple counter using JK Flip Flops.	CO3	L3	6M

UNIT-IV

8		Implement the following functions using a PLA. i) $f1(w,x,y)=\Sigma m(3,5,6,7)$ ii) $f2(w,x,y)=\Sigma m(0,2,4,7)$	CO3	L4	10M

9	**a**	Derive the PLA programming table for the combinational circuit that squares a 3-bit number.	CO4	L2	5M
	b	Compare three combinational circuits: PLA, PAL and ROM.	CO4	L1	5M

UNIT-V

10		Explain in detail different modeling styles of VHDL with suitable examples.	CO5	L2	10M

OR

11	**a**	Write a VHDL program for Full adder.	CO5	L5	5M
	b	Write a VHDL program for 3 to 8 Decoder.	CO5	L5	5M

*** END ***